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EXAMINER	
SINGH, DALIP K	

ART UNIT	PAPER NUMBER
2628	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,015	DIAMOND ET AL.	
	Examiner	Art Unit	
	Dalip K. Singh	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's amendment dated January 25, 2006, in response to PTO Office Action dated October 7, 2005. The amendments to claim(s) 1, 3, 4, 5; and the addition of claim(s) 11-20 have been noted and entered in the record, and applicant's remarks have been carefully considered resulting in the action as set forth herein below.

2. Applicant's arguments filed January 25, 2006, with respect to the rejection(s) of claim(s) 5-9 under U.S. 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of U.S. 6,555,745 B1 to Kruse et al.

Claim Rejections - 35 USC § 112

3. Claim 13 recites the limitation "the edge connector" in line 2. There is insufficient antecedent basis for this limitation in the claim.

4. Claim 17 recites the limitation "the fully-changeable graphics cards" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 6, 8, 9, 17, 18, 20 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al.

a. Regarding claim 1, Wilen et al. **discloses** an output device (display monitor 135, Fig. 1) interfaced to a motherboard (computer system 100, Fig. 1); a fixed rendering device (on-board accelerated graphics port (AGP) device 150, Fig. 1) mounted to the motherboard (computer system 100) for generating information to be output on said output device (display monitor 135); a connector (AGP connector 152, Fig. 1) for attaching one of a plurality of different field-changeable graphics cards (...the external AGP device 154 is an add-on...located externally to the motherboard...The ADD card 156 is a graphics device that interfaces the AGP connector 152...col. 3, lines 34-39) including a field-changeable rendering card (external AGP device 154, Fig. 1) to the motherboard (computer system 100), the connector comprising a plurality of connector pins (...The AGP connector 152 is a connector that supports the AGP standard (e.g., version 2.0)...col. 3, lines 25-35). Wilen et al. **does not explicitly disclose** a detection circuitry for detecting that a field-changeable rendering card housing a discrete rendering device is coupled to said connector, however, it **does disclose** the external AGP device 154 as an add-on graphics device located externally to the motherboard and an ADD card 156 that interfaces to the AGP connector 152 (...The external AGP device 154 is an add-on AGP-compatible graphics device located externally to the motherboard. The ADD card 156 is a graphics device that interfaces to the AGP connector 152...col. 3, lines 34-37). Further, Wilen et al. **discloses** a strapping scheme that indicates the presence of ADD card 156 at the AGP connector housing (...One way to do this is to use a pull-up resistor at the PAR signal....To indicate that an ADD card is used, the aDD card pulls this signal LOW...col. 6, lines 49-52;...the configuration signals ADD_ID0 to ADD_ID7 are strapped to high or low depending on the configuration of the ADD

card 156...col. 6, lines 60-62;...A detector pin strappable to a logic level to indicate an external graphics card is used...Abstract). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to make use of the same strapping scheme to detect presence of ADD card 156 for AGP device 154 **because** it provides an upgrade path for graphics capability if the internal graphics controller is not sufficient adding more user flexibility.

b. Regarding claim 2, Wilen et al. **discloses** wherein said fixed rendering device (on-board AGP device 150) is an integrated graphics processor (...device 150 is a graphic device...and is located on the motherboard that contains the processor 110...col. 3, lines 25-35) and said discrete rendering device is a discrete graphics processing unit (...the external AGP device 154 is an add-on...graphics device located externally to the motherboard...col. 3, lines 34-40).

c. Regarding claim 6, Wilen et al. **discloses** an external TMDS/LVDS device 142 that is an add-on card to the interface port 30.

d. Regarding claims 8 and 9, Wilen et al. **discloses** wherein said graphics processing unit is adapted to generate low voltage differential signaling (LVDS), digital video interface (DVI), television (TV) and video graphics array (VGA) signals (...the description of invention is directed to the digital video output...the invention can be practiced for other graphic modes...the DVO mode may include a digital video interface (DVI)...or low voltage differential signaling (LVDS)...the television set 146 receives the video signal...col. 2, lines 1-67; col. 3, lines 1-40).

e. Regarding claim 17, Wilen et al. **discloses** the interface port 130 includes multiplexed pins to support at least two graphics modes (col. 1, lines 10-25; col. 2, lines 62-67).

f. Regarding claim 18, Wilen et al. **discloses** wherein the connector is configured to allow a user of a computing device to replace a graphics system post-assembly (...the AGP connector 152 is a connector that supports the AGP standard...the external AGP device 154 is an add-on AGP-compatible graphics device located externally to the motherboard...col. 3, lines 30-37;...in many systems that use the integrated chipset 205, the AGP connector 152 (Fig. 1) is linked to the AGP interface 226 to provide a graphics upgrade path...col. 4, lines 39-49).

g. Regarding claim 20, Wilen et al. **discloses** a detector pin strappable to a logic level to indicate an external graphics card being used in the first graphics mode (Abstract).

h. Regarding claim 21, Wilen et al. **discloses** the interface port 120 including multiplexed pins to support at least two graphics modes. Although, Wilen et al. specifically does not disclose a first and second voltage level, it would have been obvious to a person of ordinary skill in the art at the time invention was made to make use of multiplexed pins to differentiate the presence of a graphics upgrade and a loop-thourgh card **because** it provides for graphics card selection without user intervention resulting in more efficient operations.

7. Claims 3 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al. as applied to claim 1 above and further in view of U.S. 2004/0228365 A1 to Kobayashi.

a. Regarding claim 3, Wilen et al. **is silent about** PCI express signal usage between said graphics processing unit from said integrated graphics processor in order to generate a plurality of signals for display on said output device. Kobayashi **discloses** an add-in graphics card supplanting the onboard graphics

engine (See Fig. 23) and use of PCI express port (...the PCI express port is augmented to become compliant with the requirements of the cross platform interface which can directly drive a display device...a add-in graphics card can supplant the onboard graphics engine as shown in Fig. 23...page 9; paragraph 95, 96). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen et al. with the feature "PCI Express technology for communications between on-board and external add-on graphics controllers" as taught by Kobayashi **because** PCI Express is a high-bandwidth, low pin count that maintains software compatibility with existing PCI infrastructure (page 9, paragraph 95).

b. Regarding claim 16, it is similar in scope to claim 3 above and is rejected under the same rationale.

8. Claims 4, 5, 7-9, 11, 12, 13, 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al. as applied to claim 1 above and further in view of U.S. 6,555,745 B1 to Kruse et al.

a. Regarding claim 5, Wilen et al. **is silent about** wherein said field-changeable card does not house a discrete rendering device and comprises a passive loop-through card enabling the implementation of LVDS features in the apparatus. The detailed specification of the instant application discloses how the loop-through card 650 completes the circuit paths between the output signals and LVDS panel input signals (paragraph 0030). Kruse et al. **discloses** a flexible interconnect arrangement (FIA) facilitating low voltage differential signal communications between an analyzer and a display screen with a highly flexible, high impedence circuit board (col. 2, line 64-67), which acts as a loop-through card. Therefore, it would have been obvious to a person of ordinary skill in the

art at the time invention was made to modify Wilen et al. with the circuit board that enables LVDS communications **because** it provides for a reduced electromagnetic interference operations resulting in improved operations.

b. Regarding claim 7, Wilen et al. as modified by Kruse et al. **discloses** FIA 100 electrically connecting a programming unit display screen with an analyzer thus completing circuit paths (col. 3, lines 20-40).

c. Regarding claims 8 and 9, Wilen et al. **discloses** wherein said graphics processing unit is adapted to generate low voltage differential signaling (LVDS), digital video interface (DVI), television (TV) and video graphics array (VGA) signals (...the description of invention is directed to the digital video output...the invention can be practiced for other graphic modes...the DVO mode may include a digital video interface (DVI)...or low voltage differential signaling (LVDS)...the television set 146 receives the video signal...col. 2, lines 1-67; col. 3, lines 1-40).

d. Regarding claim 11, Wilen et al. as modified by Kruse et al. **discloses** detection of mode of operation by the connector pins (...The ADD-Detect signal is used to identify that the ADD card 156 is used instead of the AGP card 154...one way to do this is to use a pull-up resistor at the PAR signal...col. 6, lines 40-65: Wilen); a flexible interconnect arrangement (FIA) facilitating low voltage differential signal communications between an analyzer and a display screen with a highly flexible, high impedence circuit board (col. 2, line 64-67), which acts as a loop-through card.

e. Regarding claim 4, Wilen et al. **discloses** wherein said graphics processing unit is adapted to generate low voltage differential signaling (LVDS), digital video interface (DVI), television (TV) and video graphics array (VGA) signals (...the description of invention is directed to the digital video output...the

invention can be practiced for other graphic modes...the DVO mode may include a digital video interface (DVI)...or low voltage differential signaling (LVDS)...the television set 146 receives the video signal...col. 2, lines 1-67; col. 3, lines 1-40).

f. Regarding claim 12, Wilen et al. as modified by Kruse et al. **discloses** wherein the connector is adapted to cause an LVDS signal to be routed through the loop-through card to the output device comprising a display (...a first end 102 of flexible interconnect arrangement 100 connects to the display screen via a connector 103. A second end 104 connects to the analyzer of the programming unit via a connector 105...col. 3, lines 20-40), the loop-through card being a conduit for passing the signals through without any processing to the display.

g. Regarding claim 13, Wilen et al. as modified by Kruse et al. **discloses** wherein a passive loop-through and the edge connector is adapted to receive a plurality of DVI signals on several of the plurality of connector pins and route the DVI signals thorough the loop-through card to the output device (...the interface port 130 provides connection pins to interface to a number of devices...the DVO mode may include a digital visual interface (DVI) which supports TMDS or LVDS devices...col. 2, lines 62-67; col. 3, lines 1-3), the loop-through card being a conduit for passing the signals through without any processing to the display.

h. Regarding claim 14, Wilen et al. as modified by Kruse et al. **discloses** an example of the data processing arrangement including an implanted medical device programming unit that uses flexible interconnect arrangement (FIA) 100 to electrically connect a programming unit display screen with an analyzer of the programming unit (col. 3, lines 22-27). Although Kruse et al. **does not disclose** a discrete rendering device, it would have been obvious to a person of ordinary skill in the art at the time invention was made to include such a rendering device

in the flexible interconnect arrangement (FIA) **because** it would result in a more stable graphics output with less noise introduced due to longer data path that graphics signal has to travel.

i. Regarding claim 15, it is similar in scope to claim 14 above and is rejected under the same rationale.

9. Claims 10 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,724,389 B1 to Wilen et al. as applied to claim 1 above and further in view of U.S. 6,893,268 B1 to Harari et al.

a. Regarding claim 10, Wilen et al. **does not disclose** wherein said field-changeable rendering card is an audio chip. Harari et al. **discloses** a removable mother/daughter peripheral card capable of processing audio (...the optional functional component 42 includes a data decompression module for decompressing...audio data..col. 13, lines 1-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen with the feature "audio processing module on a mother/daughter peripheral card" as taught by Harari et al. **because** it provides the user flexibility to upgrade audio performance.

b. Regarding claim 19, Wilen et al. **does not disclose** wherein the graphics card is maintained in a substantially parallel, spaced apart relation relative to the motherboard. Harari et al. **discloses** in Fig. 1 how the removable mother card 100 is adapted to host system 200 and the Fig. 1 shows that mother card is parallel to the host system. Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Wilen et al. with the feature "graphics card is in parallel spaced apart

relation" as taught by Harari **because** it results in a compact footprint which results in space savings on a mother board.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(571) 272-7792**. The examiner can normally be reached on Mon-Friday (10:00AM-6: 30PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Ulka Chauhan**, can be reached at **(571) 272-7782**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, please contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). Please note that the new Central Official FAX number for application specific communications with the USPTO is **571-273-8300** (effective July 15, 2005).

Dalip K. Singh

Examiner, Art Unit 2628

dks

August 23, 2006

ULKA CHAUHAN
SUPERVISORY PATENT EXAMINER